Data Sheet

Universal counter IC 7226A

RS stock number 304-138

The RS 7226A universal counter IC is a fully integrated 8-digit universal counter with the same features as the RS 7216A. In addition multiplexed BCD outputs and control signals to aid transfer of measured information to other devices are included. Contained in the device is a high frequency oscillator, decade timebase counter, an 8-decade data counter with latches and a 7 segment decoder and digit multiplexer with segment and digit drivers to directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in the frequency and unit counter modes and 2MHz in the other (period, frequency ratio and time interval) modes. Both inputs have digital input characteristics.

Absolute maximum ratings

Maximum supply voltage (V^+) _____ 6.5V
Maximum digit output current _____ 400mA
Maximum segment output current _____ –60mA
Voltage on any input or output terminal (1) _____ V+ +0.3 to -0.3V
Maximum power dissipation at 70° C _____ 1.0W
Maximum operating temperature range _____ –20°C to +70°C
Maximum storage temperature range _____ –55°C to +125°C

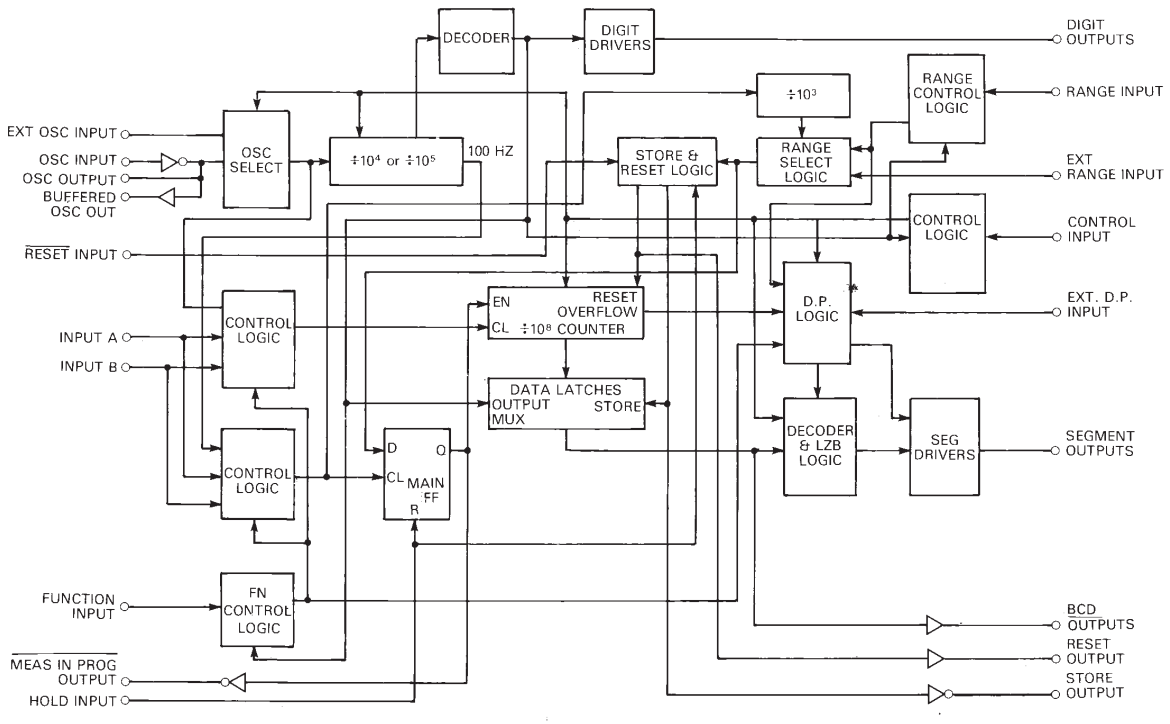
Features

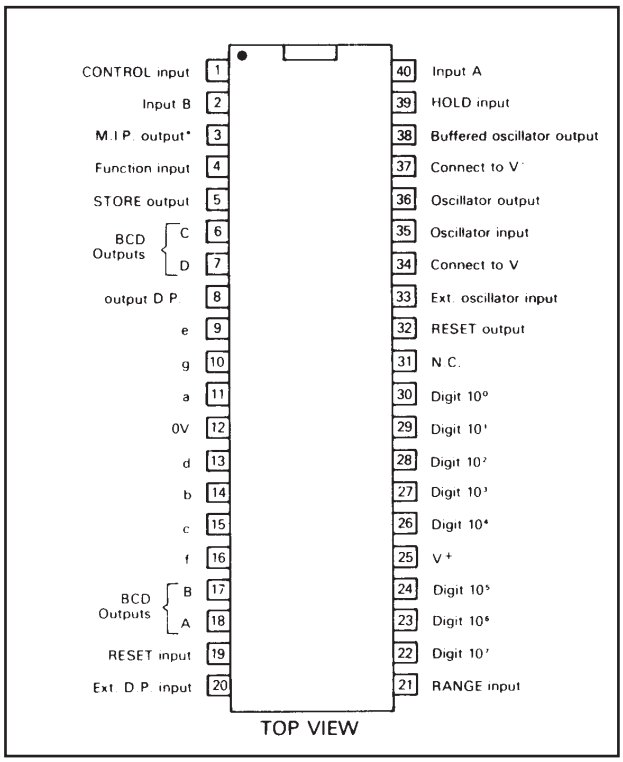
- Four internal gate times: 0.01 sec, 0.1 sec, 1 sec, 10 sec in frequency counter mode
- 1 cycle, 10 cycles, 100 cycles, 1000 cycles in period, frequency ratio and time interval modes
- Measures frequencies from d.c. to 10MHz
- Measures period from 0.5µ sec to 10 sec
- Eight digit multiplexed LED outputs
- Multiplexed BCD outputs
- Control signals to aid data transfer
- Output drivers will directly drive both digits and segments of large LED displays
- Stable high frequency oscillator, uses either 1MHz or 10MHz crystal
- Internally generates multiplex timing with inter-digit blanking, leading zero blanking and overflow indication
- Decimal point and leading zero blanking controlled directly by the chip
- All terminals protected against static discharge.

Note:

1. The RS 7226A may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ by more that 0.3V.

Figure 1 **Block diagram**





General notes

Inputs A & B

Inputs A and B are digital inputs with a typical switching threshold of 2.0V at V^+ = 5.0V. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transition at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed inputs

The function, range and control inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output (typically 125µsec). The multiplex inputs are active high for a common anode display.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED's to the multiplex inputs. For a maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs and a 68pF capacitor to decouple the inputs to 0V as shown in Figure 10.

Table 1 shows the functions selected by each digit for these inputs.

Control input functions

Display test - All segments are enabled continuously giving a display of all 8's with decimal points. The display will be blanked if display off is selected at the same time.

Display off - To enable the display off mode it is necessary to connect $D10^3$ to the control input and have the HOLD input at V^+. The chip will remain in the display off mode until HOLD is switched back to 0V. While in the display off mode, the segment and digit driver outputs are open. During display off the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initialised when the HOLD input is switched to 0V.

1MHz enable - The 1MHz enable mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in µsec increments rather than 0.1 µsec increments.

External oscillator enable - In this mode the external oscillator input is used instead of the on-chip oscillator for timebase input and main counter input in period and time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself to enable the on-chip oscillator. (The **RS** 10MHz crystal oscillator is ideally suited as an external oscillator).

Table 1

	Function	Digit
FUNCTION INPUT Pin 4	Frequency	$D10^0$
	Period	$D10^7$
	Frequency Ratio	$D10^1$
	Time Interval	$D10^4$
	Unit Counter	$D10^3$
	Oscillator Frequency	$D10^2$
RANGE INPUT Pin 21	.01 sec/1 hertz	$D10^0$
	0.1 sec/10 hertz	$D10^1$
	1 sec/100 hertz	$D10^2$
	10 sec/1k hertz	$D10^3$
CONTROL INPUT Pin 1	Blank Display	$D10^3$ and HOLD
	Display Test	$D10^7$
	1 MHz Enable	$D10^1$
	External Oscillator	$D10^0$
	External D.P. Enable	$D10^2$
EXTERNAL DECIMAL POINT INPUT Pin 20	Decimal Point is output for same digit that is connected to this input.	

Electrical characteristics T_A = 25˚C, V^+ = 5.0V, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating supply current	I_{DD}	Display off, unused inputs to 0V		2	5	mA
Supply voltage range		–20˚C<T_A<+70˚C. Input A, Input B frequency at F_{MAX}	4.75		6.0	V
Maximum frequency Input A, Pin 40	F_{AMAX}	–20˚C<T_A<+70˚C 4.75<V^+<6.0V, Figure 2 Function = frequency, ratio, unit counter	10			MHz
		Function = period, time interval	2.5			MHz
Maximum frequency Input B, Pin 2	F_{BMAX}	–20˚C<T_A<+70˚C 4.75<V^+<6.0 Figure 16	2.5			MHz
Minimum separation Input A to input B Time interval function		–20˚C<T_A<+70˚C 4.75V<V^+<6.0V Figure 16	250			ns
Maximum osc. freq. and ext. osc. frequency		–20˚C<T_A<+70˚C 4.75V<V^+<6.0V	10			MHz
Minimum ext. osc. frequency					100	kHz
Multiplex frequency	$f_{max.}$	f_{osc} = 10MHz		500		Hz
Time between measurements		f_{osc} = 10MHz		200		ms
Input voltages: Pins 2, 19, 33, 39, 40		-20˚C<T_A<+70˚C				
Input low voltage	V_{IL}				1.0	V
Input high voltage	V_{IH}		3.5			V
Input resistance to V^+ Pins 19, 33	R	V_{IN} = V^1 – 1.0V	100	400		KΩ
Input leakage to Pins 2, 39,40	I_L				2.0	µA
Digit driver: Pins 22, 23, 24, 26, 27, 28, 29, 30						
High output current	I_{OH}	V_{OUT} = V^+ -2.0	150	180		mA
Low output current	I_{OL}	V_{OUT} = +1.0V		-0.3		mA
Segment driver: Pins 8, 9, 10, 11, 13, 14, 15, 16						
Low output current	I_{OL}	V_{OUT} = +1.5V	25	35		mA
High output current	I_{OH}	V_{OUT} = V^+-2.5V	100		µA	
Multiplex inputs: Pins 1, 4, 20, 21						
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Input resistance to 0V	R	V_{IN} = +1.0V	50	100		kΩ

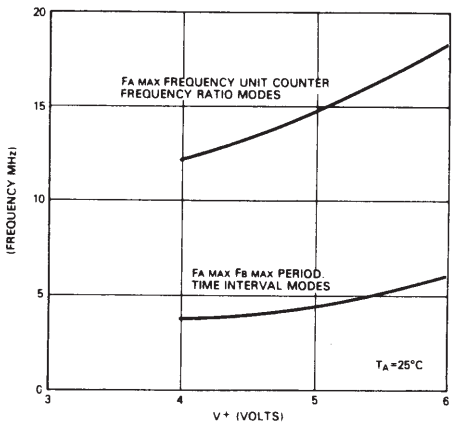
Range input - The range input selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter. In all functional modes except unit counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the range input is changed.

N.B. Readings displayed in kilohertz or microseconds.

Function input - The six functions that can be selected are: *Frequency, period, time interval, unit counter, frequency, ratio and oscillator frequency.* These functions select which signal is counted into the main counter and which signal is counted by the reference counter as shown in Table 2. In time interval a flip flop is toggled by a 1-0 transition of input A than by a 1-0 transition of input B. The oscillator is gated into the main counter from the time input A toggles the flip flop until B gates the flip flop. (For complete descriptions of workings of the time interval see later section Figure 14.) A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the function input is changed.

Table 2		
Description	**Main Counter**	**Reference Counter**
Frequency (F^A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (T^A)	Oscillator	Input A
Ratio (FA/FB)	Input A	Input B
Time Interval (A-B)	Osc (Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq.	Oscillator	100 Hz(Oscillator ÷ 10^5 or 10^4)

Figure 2 **Typical operating characteristics F_{AMAX} F_{BMAX} V_S. V^+**



Hold input - Except in the unit counter mode when the hold input is at V^+ any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updates so the last complete measurement is displayed. In unit counter mode when the hold input is V^+ the counter is stopped but not reset. When HOLD is changed to 0V, a new measurement is initiated.

Rest input - The RESET is the same as the hold input, except the latches for the main counter are enabled, resulting in an output of all zeros.

Measurement in progress, store and reset outputs - These outputs are provided to aid data transfer. Figure 3 shows the relationship between these signals during the time between measurements. All three can drive a low power schottky TTL load. The measurement in progress output can directly drive an ECL load if the two devices are on the same power supply.

BCD outputs - The BCD representation of each digit output is available at the BCD outputs as shown in Table 3. The positive going digit drivers lag the BCD data. Each BCD output will drive one low power schottky TTL load and when interfacing low power schottky TTL latches, it is necessary to use 1kΩ pull down resistors on the TTL inputs for optimum results. The display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

Figure 3 **Reset, store and measurement in progress outputs between measurements**

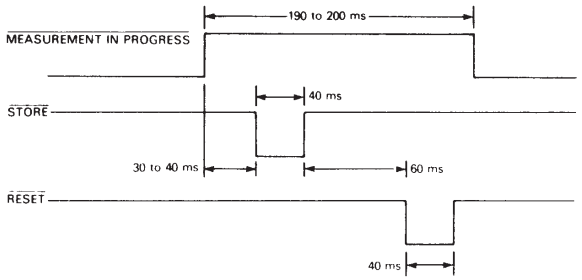


Table 3 Truth Table BCD Outputs				
Number	D Pin 7	C Pin 6	B Pin 17	A Pin 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Buffered oscillator output - The buffered oscillator output has been provided to enable used of the on-chip oscillator signal without loading the oscillator itself. This output will drive one low power schottky TTL load. Care should be taken to minimise capacitive loading on this pin.

Display considerations

The display is multiplexed at a 500Hz rate with a digit time of 244µsec. An interdigit blanking time of 6µsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the main counter overflows.

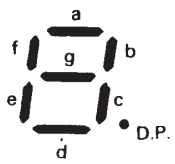
The RS 7226A is designed to drive common anode LED displays at peak current 25mA/segment, using displays with V_F = 1.8V at 25mA. The average dc current will be over 3mA under these conditions. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4 and 5 show the digit and segment currents as a functions of output voltage.

(V_{out} referred to 0V.)

To obtain additional brightness from the displays V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in the RS 7226A are not directly compatible with either TTL or CMOS logic. Should logic signals be required, the BCD outputs are available.

Segment identification:



N.B. The correct display to use with this device is a common anode with right hand decimal point eg. RS multiplexed seven segment display (**RS** stock no. 249-7816).

Figure 4 **Typical I_{DIG} V_s. $V^+ - V_{OUT}$ ($4.5V<V^+<6.0V$)**

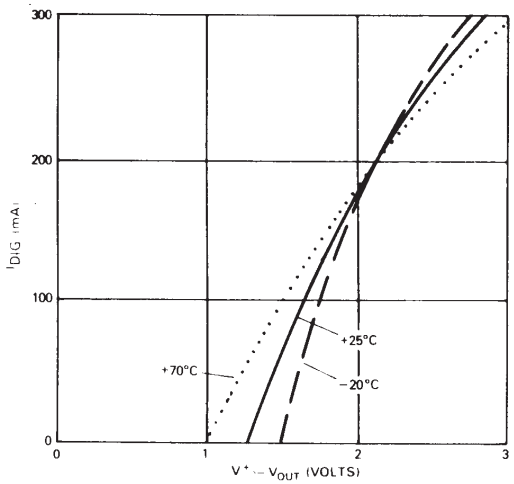


Figure 5 **Typical I_{SEG} V_s. V_{OUT} (V^+ varied)**

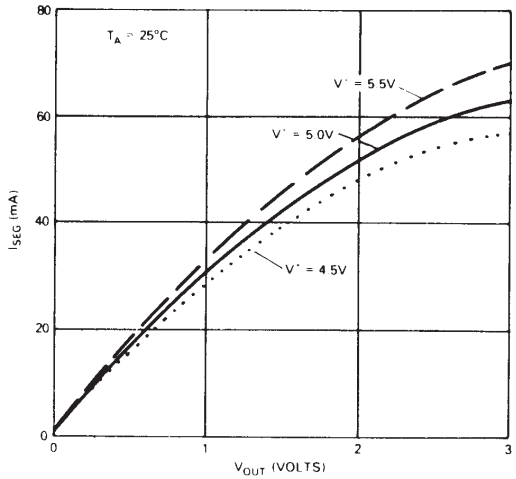
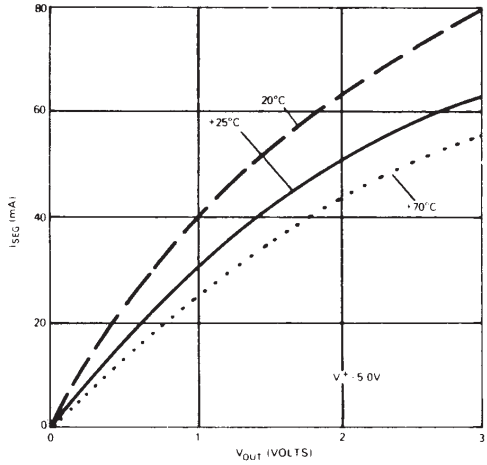


Figure 6 **Typical ISEG Vs. VOUT (temperature varied)**



Accuracy

In a universal counter crystal drift and quantisation errors cause errors. In frequency, period and time interval modes, a signal derived from the oscillator is used in either the reference counter or main counter.

Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantisation error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the frequency mode the maximum accuracy is obtained with high frequency inputs and in period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 7 the least accuracy will be obtained at 10kHz. In time interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 8. A frequency ratio measurement can be more accurately obtained by averaging over more cycles of input B as shown in Figure 9.

Figure 7 **Maximum accuracy of frequency and period measurements due to limitations of quantisation errors**

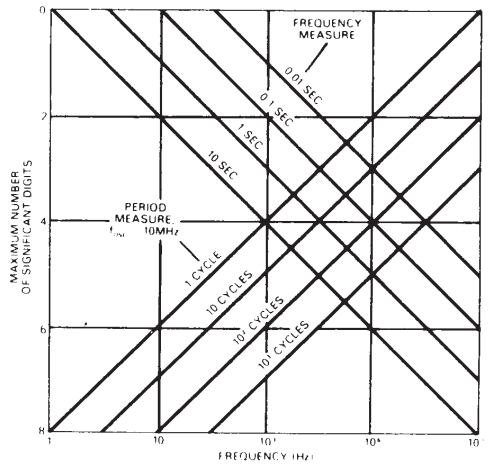


Figure 8 **Maximum accuracy of time interval measurement due to limitations of quantisation errors**

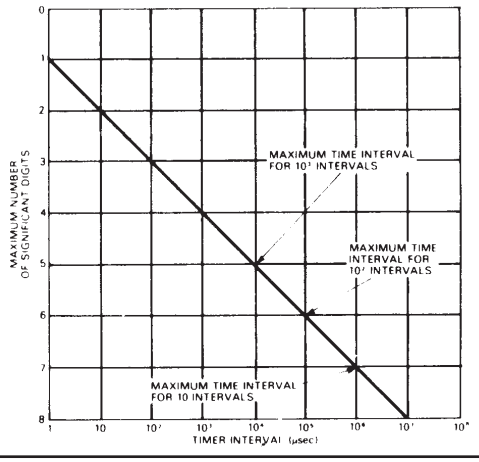
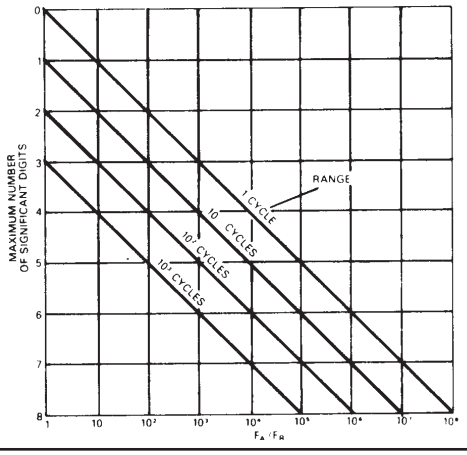
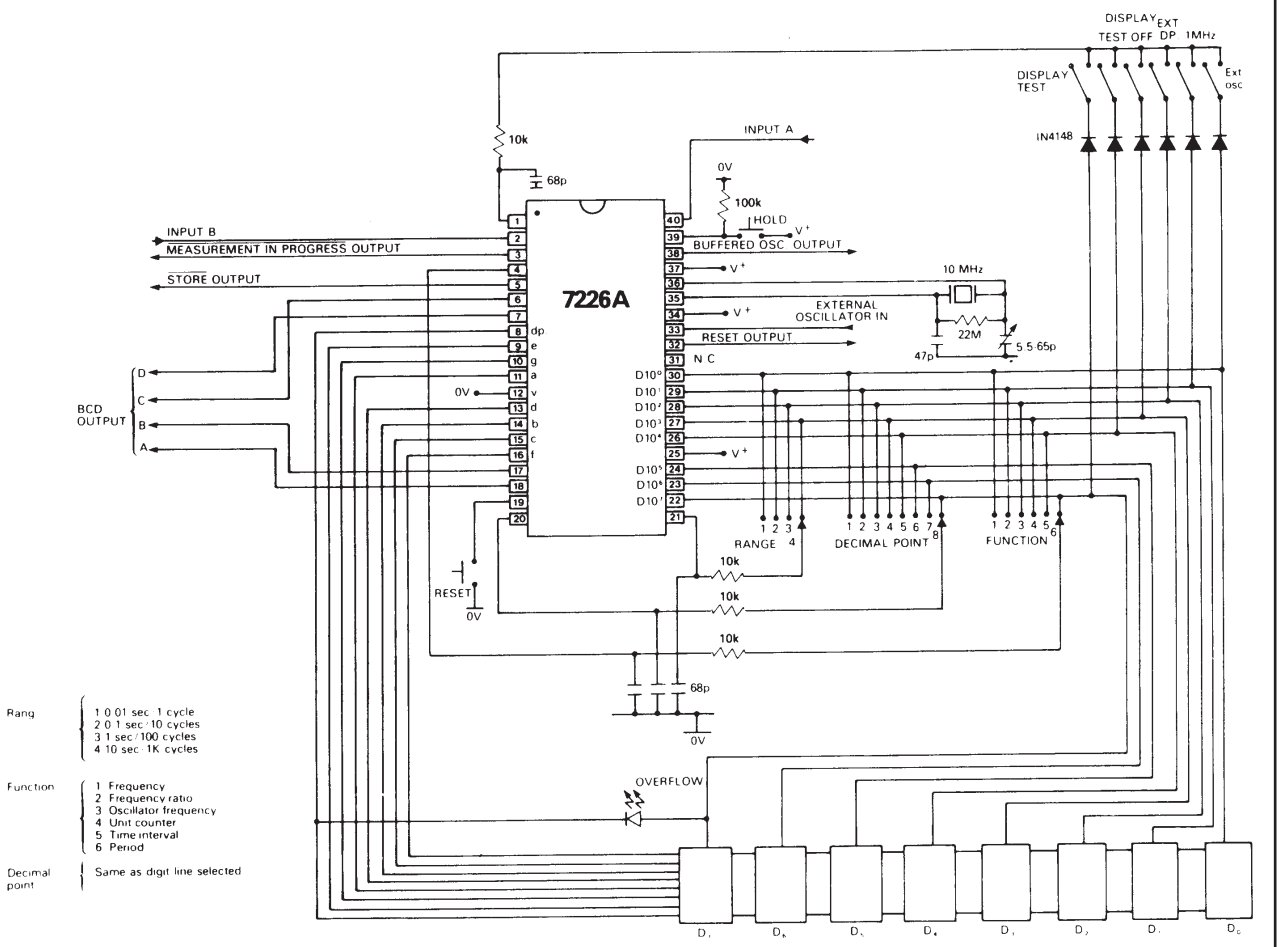


Figure 9 **Maximum accuracy for frequency ratio measurement due to limitation of quantisation errors**



Circuit applications

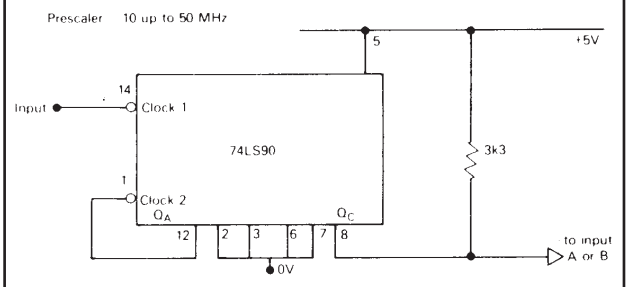
Figure 10 Circuit diagram simplest form



The RS 7226A has been designed for use in a wide range of universal counter applications. In many cases, prescalers will be required to reduce the input frequencies to under 10MHz. Because input A and B are digital inputs, additional circuitry will often be required for input buffering, amplification, hysteresis, and level shifting to obtain a good digital signal. The complexity for doing this can vary widely depending on the sensitivity and maximum frequency required.

Prescaler techniques

Figure 11 **Divide by ten prescaler**



For a full function universal counter two of these prescaler circuits will be required. Note that the input to the 74LS90 must be a digital circuit. If decimal point position correction is required see following section.

Note. The output from the 74LS90 comes from Q_C rather than Q_D to obtain an input duty cycle of 40%. If the signals at inputs A or B have very low duty cycles it may be necessary to use a monostable (74LS123 or similar) to stretch the pulse width to guarantee a 50ns minimum pulse width.

As with the ÷ 10 circuit above, two of these +100 prescaler circuits will be required for a full function counter.

External decimal point input

The external decimal point input is active when the control input (pin 1) is connected to the $D10^2$ digit line (pin 28). The decimal point input is then used to select the required decimal point position by connecting the digit strobe line for the required position to this input. The $D10^7$ (pin 22) should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This feature is extremely useful when prescalers are used and a different decimal point position is required.

Time interval mode

The principal of operation of the time interval measurement is that the counter is started by channel A going negative and after the selected number of periods is stopped by channel B going negative. However the first pair of negative edges steers the circuit into this mode of operation and therefore when single shot measurements are to be made it is necessary to ''prime'' the circuit by negative going A input followed by a negative going B input (separated by at least 250ns and complying with the specified input characteristics as shown in Figure 16).

The priming procedure may be accomplished using the circuit shown in Figure 12, but note that it may be necessary to reset the counter before priming. After ''priming'', the circuit will count the selected number of periods and display the result as an ''average''. This priming circuit has no effect on the operation of the universal counter in other modes and may therefore be left permanently connected.

N.B. ''Priming'' is not necessary if a repetitive measurement is to be made.

Accurate resolution for time interval measurement is 100ns with a maximum time between the two events of ten seconds.

For operation in the time interval mode, range 1 (0.01 sec/1 cycle) must be selected.

Figure 14 **Priming circuit for single shot operation time interval mode**

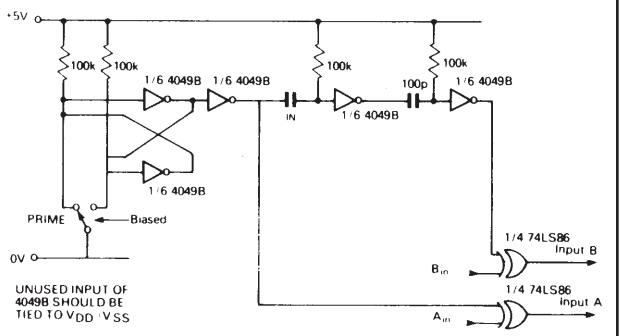


Figure 15 **Waveform for guaranteed minimum $F_{A\ MAX}$ function = frequency, frequency ratio, unit counter**

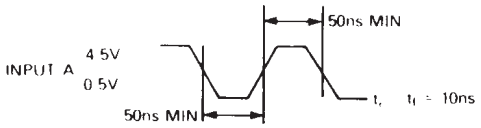
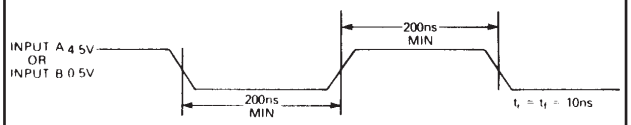


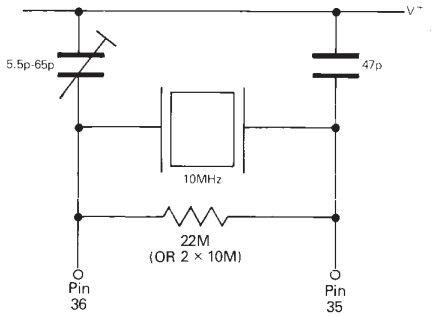
Figure 16 **Waveform for guaranteed minimum $F_{B\ MAX}$ and $F_{A\ MAX}$ for function = period and time interval**



Oscillator considerations

The easiest way of implementing the timebase oscillator is to use a 10MHz crystal (657-612) and associated circuitry as shown in Figure 17.

Figure 17 **Crystal oscillator circuit**



If the 1MHz enable option is to be used, this may be implemented simply by substituting a 1MHz crystal for the 10MHz crystal in Figure 17 and connecting the 1MHz enable control circuitry.

An external oscillator, eg. the **RS** 10MHz crystal oscillator may be used by connecting the oscillator output to pin 33 and connecting the external oscillator enable control circuitry.

N.B. Oscillator output must meet the input voltage criteria as detailed in maximum ratings and electrical characteristics sections.