Data Sheet

Thin Film Electroluminescent Graphic Displays

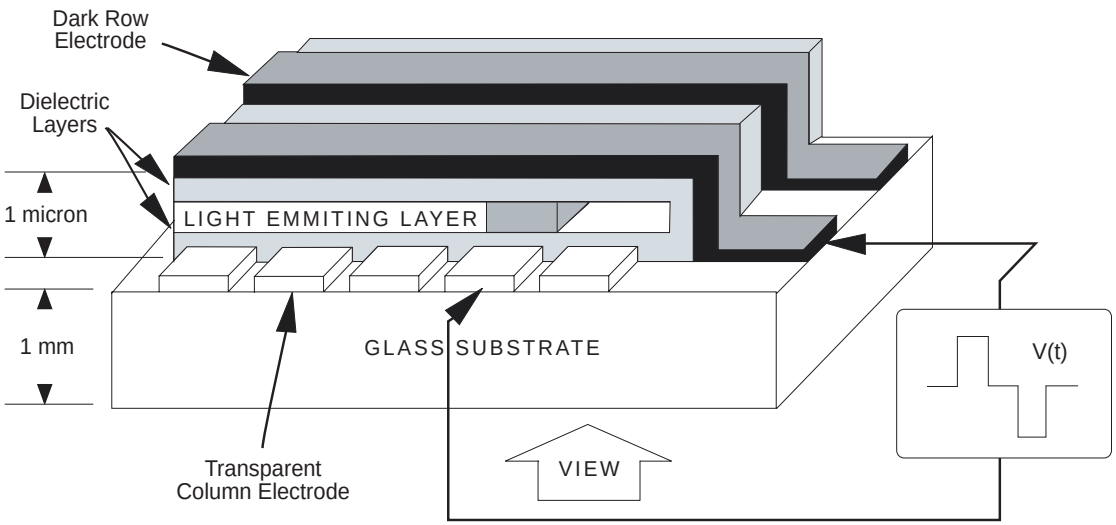
RS stock numbers 294-8601, 294-8617

Planar EL displays consist of a solid-state electroluminescent (EL) glass panel, an electronic control circuit, and a power supply.

The solid-state glass panel consists of a thin film luminescent layer sandwiched between transparent dielectric layers and a matrix of row and column electrodes.

The electronic control circuit lights pixels by energising the phosphor of intersecting rows and columns.

This solid-state process creates displays that endure extreme conditions with exceptional tolerance to shock, vibration, temperature, and humidity, while response times remain less than one millisecond.



Planar EL display architecture

	RS stock no. 294-8601	RS stock no. 294-8617
Model Name	**EL160.80.50**	**EL320.240.36**
Matrix (col x Row)	160 x 80	320 x 240
Pixel pitch in.:	0.20 x 0.020	0.014 x 0.014
W x H mm:	0.50 x 0.50	0.36 x 0.36
Viewing Area in.:	3.2 1.6 (3.6)	4.5 x 3.4 (5.6)
W x H (diag) mm:	80 x 40 (89)	115 x 86 (143)
Outline dimensions in.:	4.3 x 2.3 x 0.8	5.8 x 4.1 x 0.8
W x H x D mm:	109 x 57 x 21	148 x 105 x 20
Liminance	872	542
cd/m^2 (fL)	$(25)^2$	$(16)^2$
Contrast ratio	48: 1	31: 1
Supply voltages (Vdc)	+5, +12	+5, +12
Typical power (W)	2.1	4.0
Operating temperature (°C) -	25 to +65	-25 to +65
Storage temperature (°C) -	40 to +85	-40 to +85
Interface type	Z	Z
Features	ICE™, extended temperature range available	quarter-VGA, ICEBrite™, extended temperature range available

Features and benefits

- Excellent visual performance:
  - High brightness and contrast
  - Wide viewing angle > 160°
- Rapid display response < 1ms
- Space efficient mechanical package
- Low EMI emissions
- Extremely rugged and durable
- Reliable, long operating life

Specifications for **RS** stock nos 294-8601 & 294-8617

Performance characteristics are guaranteed when measured at 25°C with rated input voltage unless otherwise specified.

Control basics

The EL panel is a matrix structure with column and row electrodes arranged in an X-Y formation. Light is emitted when an AC voltage of sufficient amplitude is applied at a row-column intersection. The display operation is based on the symmetric, line-at-a-time data addressing scheme.

Power

The supply voltages are shown in Table 1. All internal high voltages are generated from the display supply voltage (V_H).The logic supply voltage (V_L) should be present whenever video input signals or V_H is applied. The minimum and maximum specifications in this manual should be met, without exception, to ensure the long-term reliability of the display. Planar does not recommend operation of the display outside these specifications.

Table 1. DC input voltage requirements

Parameter	Symbol	Min	Typ	Max	Absolute Max
Logic supply voltage	V_L	4.75V	5V	5.25V	6V
Logic supply current at +5V	I_L			40 mAdc	
Display supply voltage	V_H	10V	12V	15V	15V
Supply current at +12V	I_H		0.5A	0.80 Adc	
Power consumption 5 V/12 V					
@ 60 Hz Frame Rate			2.0W	2.9W	
@ 120 Hz Frame Rate			2.7W	4.2W	
@ 240 Hz Frame Rate			4.4W	7.0W	

CAUTION: Absolute maximum ratings are those values beyond which damage to the device may occur.

Table 2. Video input requirements

Description	Min	Max	Units	Notes
Absolute input voltage range	-0.3	5.5	V	VL = 5.0V
Video logic high voltage	70%	100%	V_L	All input thresholds are CMOS
Video logic low voltage	0	20%	V_L	
Video logic input current	-10	+10	µA	
Input capacitance	-	15	pF	

There is not overcurrent protection on either the V_H or V_L inputs to protect against catastrophic faults. **RS** recommends the use of a series fuse on the 12V supply (V_H). A general guideline is to rate the fuse at 1.8 to 2 times the display maximum current rating.

Connectors

Standard data and power connector

The **RS** displays, stock nos 294-8601 and 294-8617, use the Samtec STMM-110-01-T-D or equivalent connector. The mating connector and cable are supplied with display.

Figure 1 **Data/Power connector**

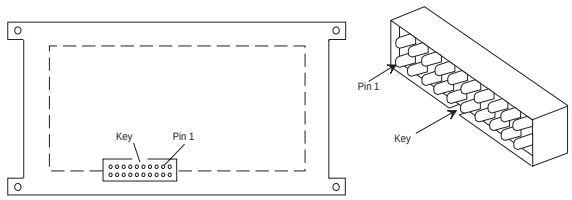


Table 3. J1 Connector pinouts

Pin	Signal	Description	Pin	Signal	Description
1	V_H	+12V Power	2	V_H	+12V Power
3	Selftest	Selftest Input [1]	4	GND	Ground
5	V_L	+5V Power	6	GND	Ground
7	VS	Vertical Sync	8	GND	Ground
9	HS	Horizontal Sync	10	GND	Ground
11	VCLK	Video Clock	12	GND	Ground
13	VID_0	Video Data	14	GND	Ground
15	VID_1	Video Data	16	GND	Ground
17	VID_2	Video Data	18	GND	Ground
19	VID_3	Video Data	20	GND	Ground

[1] Connect pin 3 to ground for normal display operation.

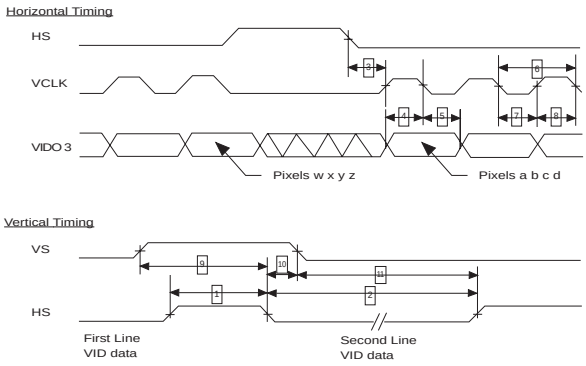
Interface information

Planar EL Small Graphics Displays (SGD) incorporate an interface that is similar to many LCD interfaces. This interface is supported by a a variety of off-the-shelf chip sets which take care of all display control functionality, freeing the system processor for other tasks. Designers select the chip set that best suits their particular architecture and price point. This 4-bit LCD-type video interface provides a low cost, flexible method for controlling display brightness and power consumption.

Video input signals

The end of the top line of a frame is marked by VS, vertical sync signal as shown in Figure 2. The end of each row of data is marked by HS. The VS signal may be independently set to a CMOS low level at any time for longer than one frame period. During the time of VS inactivity the display is blank. Halting VS results in a standby condition to minimise power usage.

Figure 2 **Video input timing diagram**



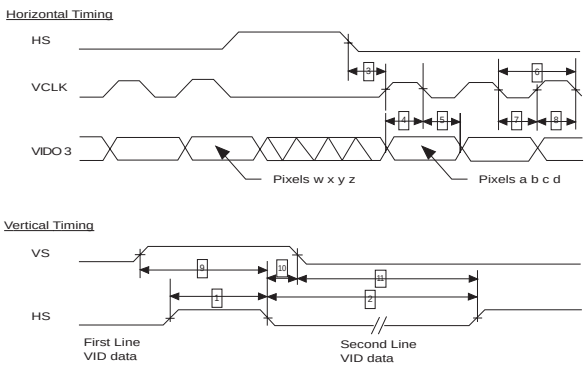
Timing is compatible with LCD graphics controllers such as the SMOS 1335, 1353 or C & T 65535.

Table 4. Video input descriptions

Num	Description	Symbol	Min.	Typ.	Max.	Units
1	HS high time	tHSh	100			ns
2	HS low time	tHSl	40			tVCLK
3	HS to VCLK rising edge	tHSsu	95			ns
4	VID setup to VCLK	tVIDsu	50			ns
5	VID hold from VCLK	tVIDhd	50			ns
6	Video clock period	tVCLK	140			ns
	VCLK rise, fall time	tVCLKrf		10	15	ns
7	VCLK low width	tVCLKl	30			ns
8	VCLK high width	tVCLKh	30			ns
9	VS high setup to HS low	tVShsu	140			ns
10	VS hold after HS	tVShd	140			ns
11	VS low setup to HS high	tVSlsu	140			ns
12	HS period	tHS	51			µs
	VS period	tVS	80			tHS
	Frame Rate	fVS	0		240	Hz

Input signals VID0 through VID3 contain the video data for the screen. Pixel information is supplied from left to right and from top to bottom four pixels at a time. Video data for one row is latched on the fall of HS.

Figure 3 **Video input timing diagram**



Self-test mode

The display incorporates a self-test mode composed of two patterns displayed for approximately two minutes each, and then repeated. The patterns are as follows; *Full ON* and *1 x 1 Checkerboard*. The self-test mode is entered by leaving pin 3 unconnected or pulled high.

Note: Pin 3 must be connected to Ground for normal display operation.

Optical

Table 5. Optical characteristics.

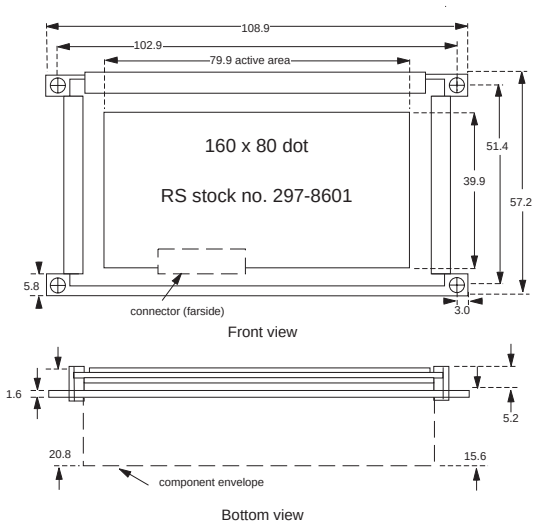
Luminance		
L_{on} (areal), min	40 cd/m2	screen centre, 120Hz frame rate
L_{on} (areal), min	78 cd/m2	screen centre, 240Hz frame rate
L_{off} (areal), max	0.3 cd/m2	3 points: centre plus two ends measured .75 ±0.25'' from adjacent display edges, @ 240Hz.
Non-uniformity		
All pixels fully lit	35%	Maximum difference between two of five points, using the formula: LNU%=[1- (min_lum/max_lum)] x 100%
Luminance variation (temperature)		
Maximum	±20%	Across operating temperature range
Luminance variance (time)		
Maximum	<20%	10,000 hours at 25°C ambient
Viewing Angle		
Minimum	160°	
Contrast ratio		
Typical	50:1	@500 lux ambient, 240Hz frame rate

Dimming

There are two standard methods for dimming the display. Frame rate dimming allows the brightness of the display to be lowered proportionally by reducing the frame rate. Frame rate dimming is performed within the application by lowering the frame rate of the video input signals. Because brightness is proportional to frame rate, the display can be dimmed by adding pauses between every horizontal period.

The lowest useable frame rate (brightness) is dependent on the perceived flicker of the displayed image, but will most likely be around 60Hz.

Figure 4



Installation and Handling

Do not drop, bend, or flex the display. Do not allow objects to strike the surface of the display.

CAUTION: The display uses CMOS and power MOS-FET devices. These components are electrostatic sensitive. Unpack, assemble, and examine this assembly in a static-controlled area only When shipping, use packing materials designed for protection of electrostatic-sensitive components.

Mounting EL displays

Properly mounted, EL displays can withstand high shock loads as well as severe vibration found in demanding applications. However the glass panel used in an EL display will break if subjected to bending stresses, high impact, or excessive loads.

Avoid bending the display. Stresses are often introduced when a display is mounted into a product. Ideally, the mounting tabs of the display should be the only point of contact with the system. Use a spacer or boss for support; failure to do so will bend the display and cause the glass to break. The instrument enclosure or frame should not flex or distort in such a way that during use the bending loads might be transferred to the display. Mounting surfaces should be flat to within ±0.6mm (±0.25″). Use all the mounting holes provided. Failure to do so will impair the shock and vibration resistance of the final installation.

CAUTION: Properly mounted, this display can withstand high shock loads and severe vibration in aggressive environments. However, the glass panel used in this display will break when subjected to bending stresses, high impact, or excessive loads.

To prevent injury in the event of glass breakage, a protective overlay should be used on the viewer side of the display.

WARNING: These products generate voltages capable of causing personal injury (high voltage up to 235Vac). Do not touch the display electronics during operation.

Cable length

A maximum cable length of 600mm (24in) is recommended. Longer cables may cause data transfer problems between the data transmitted and the display input connector. Excessive cable lengths can pick up unwanted EMI. There are third party products which allow this maximum cable length to be exceeded.

Cleaning

As with any glass or coated surface, care should be taken to minimise scratching. Clean the display glass with mild, water-based detergents only. Apply the cleaner sparingly to a soft cloth, then wipe the display. Disposable cleaning cloths are recommended to minimise the risk of inadvertently scratching the display with particles embedded in a re-used cloth. Particular care should be taken when cleaning displays with anti-glare and anti-reflective films.

Avoiding burn-in

As with other light emitting displays, use a screen saver or image inversion to avoid causing burn-in on the display. Displaying fixed patterns on the screen can cause burn-in, where luminance variations can be noticed.